1. (Amended) A multilevel metal interconnect formed on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, a patterned metal layer including a plurality of metal lines, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers; and

a dielectric structure formed between laterally adjacent metal lines of a patterned metal layer, the dielectric structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material.

2. (Amended) The multilevel metal interconnect of claim 1 and further comprising a plurality of trenches formed in the layers of insulation material, each trench adjoining metal lines of the top patterned metal layer, a trench extending from the top metal layer between metal lines of the top metal layer through the top insulation layer and between metal lines of a metal layer lying below the top metal

Contd A1

layer, each trench having a bottom surface, the trenches not including conductive material.

SUB B1

5. (Amended) The multilevel metal interconnect of claim 2 wherein the bottom surface of the trench is spaced apart from a top surface of the semiconductor substrate.

A2

6. (Amended) A multilevel metal interconnect formed on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers; and

a capacitive structure formed between adjacent metal lines of a patterned metal layer, the capacitive structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material, the dielectric material including a plurality of layers of dielectric material.

SUB B1

7. (Amended) The multilevel metal interconnect of claim 1 wherein the dielectric structure has a layer of material formed to adjoin a layer of insulation material, the layer of material being different from the layer of insulation material.

8. (Amended) The multilevel metal interconnect of claim 2 wherein the dielectric structure is formed adjacent to a trench.

9. (Amended) The multilevel metal interconnect of claim 2 wherein the dielectric structure is formed between a pair of adjacent trenches.

Cont'd A2

10. (Amended) A multilevel metal interconnect formed on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers;

a capacitive structure formed between adjacent metal lines of a patterned metal layer, the capacitive structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material; and

a plurality of trenches formed in the layers of insulation material, a first trench being filled with air and a second trench being filled with the capacitive structure.

Please add the following new claims:

--26. A multilevel metal interconnect comprising:

a first plurality of metal lines that lie in substantially a same horizontal plane, the first plurality of metal lines including first, second, and third metal lines, the first, second, and third metal lines each having a top surface, a bottom surface, and side wall surfaces that contact the top and bottom surfaces;

a first dielectric that contacts the first metal line and the second metal line; and

a second dielectric that contacts the second metal line and the third metal line, the second dielectric being different from the first dielectric.

27. The multilevel metal interconnect of claim 26 wherein the first dielectric contacts a side wall of the first metal line and a side wall of the second metal line.

28. The multilevel metal interconnect of claim 27 wherein the second dielectric contacts a side wall of the second metal line and a side wall of the third metal line.

29. The multilevel metal interconnect of claim 26 wherein the second dielectric does not contact the first metal line.

SUB B7

30. The multilevel metal interconnect of claim 26 and further comprising a third dielectric that contacts the bottom surfaces of the first, second, and third metal lines.

31. The multilevel metal interconnect of claim 30 wherein the second dielectric material is formed between the third dielectric that contacts the bottom surfaces of the second and third metal lines.

32. The multilevel metal interconnect of claim 31 wherein the first dielectric and the third dielectric are different.

cont'd B3

33. The multilevel metal interconnect of claim 30 and further comprising a second plurality of metal lines that lie in substantially a same plane, the second plurality of metal lines including third, fourth, and fifth metal lines that contact the third dielectric, the third, fourth, and fifth metal lines each having a top surface, a bottom surface, and side wall surfaces.

34. The multilevel metal interconnect of claim 33 wherein the first dielectric is laterally formed between the fourth metal line and the fifth metal line.

35. The multilevel metal interconnect of claim 34 wherein the first dielectric contacts the fifth metal line.

36. The multilevel metal interconnect of claim 34 wherein the second dielectric contacts a side wall of the fifth metal line and a side wall of the sixth metal line.

37. The multilevel metal interconnect of claim 33 wherein the second dielectric does not contact the fourth metal line.

Cont'd Sub B1 A3

44. The multilevel metal interconnect of claim 43 wherein the first dielectric and the third dielectric are different.--

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38. A multilevel metal interconnect comprising:

a first plurality of metal lines that lie in substantially a same horizontal plane, the first plurality of metal lines including first, second, and third metal lines, the first, second, and third metal lines each having a top surface, a bottom surface, and side wall surfaces that contact the top and bottom surfaces;

a first dielectric that contacts the first metal line and the second metal line; and

a second dielectric that contacts the side wall of the third metal line, the second dielectric being different from the first dielectric.

Amd'd B3

39. The multilevel metal interconnect of claim 38 wherein the first dielectric contacts a side wall of the first metal line and a side wall of the second metal line.

40. The multilevel metal interconnect of claim 39 wherein the second dielectric contacts a side wall of the second metal line.

41. The multilevel metal interconnect of claim 38 wherein the second dielectric does not contact the first metal line.

42. The multilevel metal interconnect of claim 38 and further comprising a third dielectric that contacts the top surfaces of the first, second, and third metal lines.

43. The multilevel metal interconnect of claim 42 wherein the second dielectric material is formed between the third dielectric that contacts the top surfaces of the second and third metal lines.